IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device containing a multi-layered wiring structure formed on a semiconductor substrate, the structure including at least two wiring layers formed in an interlayer insulation layer, and each of the wiring layers including a metal wiring made of one of Cu and a Cu alloy;

wherein the multi-layered wiring structure comprises:

a lower wiring layer formed under the interlayer insulation layer;

a via buried in the interlayer insulation layer and connected between an upper wiring layer and a first damaged region formed on the lower wiring layer; and

a dummy via buried in the interlayer insulation layer, the dummy via being not connected to the upper wiring layer but connected to a second damaged region formed on the lower wiring layer,

wherein voids are generated at the second damaged region in the lower wiring layer of Cu or Cu alloy to cause a contact defect between the dummy via and the lower wiring layer.

Claim 2 (Previously Presented): A semiconductor device according to claim 1, wherein the dummy via is buried in the interlayer insulation layer to be connected between a dummy wiring layer and the lower wiring layer.

Claim 3 (Original): A semiconductor device according to claim 1, wherein the dummy via includes Cu buried in a via hole formed in the interlayer insulation layer.

Claim 4 (Previously Presented): A semiconductor device according to claim 1, wherein the lower wiring layer includes at least the second damaged region formed at a

portion of the lower wiring layer connected to the dummy via buried in the interlayer insulation layer.

Claim 5 (Previously Presented): A semiconductor device according to claim 4, wherein the first damaged region includes a region formed when the via hole is formed through the interlayer insulation layer.

Claim 6 (Previously Presented): A semiconductor device according to claim 1, wherein the lower wiring layer includes a portion having a width greater than that of a remaining thereof and a plurality of vias connected to the lower wiring layer are formed in the interlayer insulation film.

Claim 7 (Previously Presented): A semiconductor device according to claim 4, wherein a plurality of damaged regions connected to a plurality of dummy vias are located at a peripheral part of the lower wiring layer surrounding a contact portion of the lower wiring layer contacting with the via.

Claim 8 (Previously Presented): A semiconductor device according to claim 4, wherein the second damaged region connected to the dummy via is located away from the contact portion connected to the via on the lower wiring layer by a minimum distance defined by a design rule.

Claim 9 (Previously Presented): A semiconductor device according to claim 7, wherein the plurality of damaged regions are formed at portions of the lower wiring layer surrounding three of four sides of a location contacting with a contact portion of the via.

Claim 10 (Previously Presented): A semiconductor device according to claim 4, wherein the dummy via buried in the interlayer insulation layer includes one end contacting with the second damaged region of the lower wiring layer and the other end which is not connected with the upper wiring layer.

Claim 11 (Original): A semiconductor device according to claim 10, wherein the dummy via contains a structure similar to that of the via.

Claim 12 (Currently Amended): A semiconductor device according to claim 10, wherein the dummy wiring layer connected to the dummy via is formed on the interlayer insulation layer as a dummy wiring pattern which is not connected with the via but is connected with the dummy via.

Claim 13 (Original): A semiconductor device according to claim 12, wherein the dummy wiring layer and the upper wiring layer are formed in the same wiring layer.

Claim 14 (Currently Amended): A semiconductor device containing a multi-layered wiring structure formed on a semiconductor substrate, the multi-layered wiring structure including at least two wiring layers formed in an interlayer insulation layer, and each of the wiring layers including a metal wiring made of one of Cu and a Cu alloy;

wherein the multi-layered wiring structure comprises:

a narrow width lower wiring layer connected with a wide width lower wiring layer having a width wider than that of the narrow width lower wiring layer, the narrow width

lower wiring layer and the wide width lower wiring layer being formed in a wiring layer formed in the interlayer insulation layer;

a via buried in the interlayer insulation ~~film~~ layer to connect a first damaged region formed on the narrow width lower wiring layer with an upper wiring layer; and

a dummy via buried in the interlayer insulation layer, the dummy via being not connected to the upper wiring layer but connected to a second damaged region formed on the wide width lower wiring layer,

wherein voids are generated at the second damaged region in the wide width lower wiring layer of Cu or Cu alloy to cause a contact defect between the dummy via and the wide width lower wiring layer.

Claim 15 (Previously Presented): A semiconductor device according to claim 14, wherein the dummy via is formed in the interlayer insulation layer at a location corresponding to the second damaged region formed in a vacant region between the narrow width lower wiring layer and the wide width lower wiring layer.

Claim 16 (Previously Presented): A semiconductor device according to claim 15, wherein a dummy via contacting with the second damaged region is buried in the interlayer insulation layer.

Claim 17 (Original): A semiconductor device according to claim 14, wherein the dummy via includes a structure similar to that of the via.

Claim 18 (Original): A semiconductor device according to claim 14, wherein a dummy wiring connected to the dummy via is formed on the interlayer insulation layer as a dummy wiring pattern which is not connected with the via.

Claim 19 (Original): A semiconductor device according to claim 18, wherein the dummy wiring layer and the upper wiring layer are formed in the same wiring layer.

Claim 20 (Currently Amended): A semiconductor device comprising:

a lower wiring layer formed on a semiconductor substrate using Cu or a Cu alloy;

an interlayer insulation layer formed on the lower wiring layer;

an upper wiring layer formed on the interlayer insulation layer;

a via buried in a via hole formed in the interlayer insulation layer to be connected between the upper wiring layer and the lower wiring layer which has a first damaged region formed at a portion corresponding to the via hole; and

a dummy via buried in a dummy via hole formed in the interlayer insulation layer in a similar manner as the via hole, the dummy via being not connected with the upper wiring layer but connected with a second damaged region formed in the lower wiring layer,

wherein voids are generated at the second damaged region in the lower wiring layer of Cu or Cu alloy to cause a contact defect between the dummy via and the lower wiring layer.